

REMARKS

Summary of Examiner Interview.

Applicants hereby acknowledge the Examiner Interview between the Examiner, Alexander Williams, and Attorney for Applicants, Serge J. Hodgson, on March 1, 2005. A draft of this Amendment was presented as an exhibit to the Examiner for discussion. Agreement was not reached as to whether this Amendment places the Application in a condition for allowance.

If this Examiner believes that this Amendment does not place the Application in a condition for allowance, Applicants respectfully request that the Examiner telephone the Attorney for Applicants to resolve any outstanding issues.

Status of Claims

In the Office Action Summary, the Examiner states that Claims 21-22, 39-42, 47, 50-65 are pending in the application.

Applicants note that Claims 43-46 are pending in the Application although not included in the Examiner's listing of pending claims. Should the Examiner disagree, Applicants respectfully request the Examiner point out where Claims 43-46 were canceled.

In this amendment, Claim 65 has been canceled without prejudice. Claims 21, 39, 47, 50-53, 63-64 have been amended for purposes of clarity and thus for reasons unrelated to patentability. Support for the amendments of Claims 21, 39, 47, 50-53, 63-64 appears in the specification at least at page 4, line 7 to page 23, line 21 and in FIGS. 1 and 2.

Accordingly, after entry of this Amendment, Claims 21-22, 39-47, and 50-64 are pending in the Application.

Claims 21, 22, 39-42, 47, 50-59 and 63-65 are novel over Kondo et al. (JP2001-308262).

Kondo et al. (JP2001-308262) is not prior art under 35 U.S.C. 102(e) with respect to the present application as set forth below.

Initially, Applicants note the Examiner cites Kondo et al. at "Japan Patent # 2001-208262" at pages 3, 11 of the Office Action yet lists Kondo et al. as 2001-308262 on the Notice of References Cited, PTO-892. Further, a copy of JP 2001-308262 and a translation of the abstract of 2001-308262 was provided with Office Action. Thus, the Examiner lists in error 2001-208262 at pages 3, 11 of the Office Action and the correct citation is Kondo et al., JP 2001-308262. Applicants request clarification of the record.

The Examiner states:

Claims 21, 22, 39 to 42, 50 to 59 and 63 to 65 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kondo et al. (Japan Patent #2001-208262). (Office Action, page 3, emphasis added.)

Applicants respectfully submit that Kondo et al. (JP 2001-308262) can not be applied under 35 U.S.C. § 102(e). As set forth in MPEP 706.02(f)(1):

(A) The potential reference must be a **U.S. patent, a U.S. application publication** (35 U.S.C. 122(b)) or a **WIPO publication** of an international application under PCT Article 21(2) in order to apply the reference under 35 U.S.C. 102(e). (Page 700-27, Rev. 2, May 2004, emphasis added.)

Since Kondo et al. (JP 2001-308262) is not a **U.S. patent, a U.S. application publication** (35 U.S.C. 122(b)) or a **WIPO publication** of an international application under PCT Article 21(2), Kondo et al. (JP 2001-308262) can not be applied under 35 U.S.C. § 102(e).

Applicants further note that the date of **March 9, 2001** of the foreign application 2001-12326 upon which the present application claims priority **is prior to** the publication date of **November 2, 2001** of Kondo et al. (JP 2001-308262). Accordingly, Kondo et al. is not prior art with respect to the present application. Should the Examiner disagree, Applicants respectfully request that the Examiner set forth the basis under which Kondo et al. is prior art with respect to the present application.

Regarding the priority date for the present application, Applicants note that the Examiner states:

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15. (Office Action, page 8.)

The Examiner's statement is respectfully traversed. Applicants note that the English language translation was filed together with a statement that the translation is accurate on December 9, 2003 and received by the USPTO on December 15, 2003. Applicants further note that the English language translation together with the statement appears in the image file wrapper in the PAIR system demonstrating that the documents were received by the USPTO. Should the Examiner need an additional copy of the documents or a copy of the USPTO date stamped return receipt postcard documenting receipt by the USPTO, please contact the undersigned attorney for Applicant.

Accordingly, **the present application is entitled to claim priority to March 9, 2001**, the filing date of foreign application 2001-12326 upon which the present application claims priority.

Thus, Claims 21, 22, 39-42, 47, 50-59 and 63-65 are novel over Kondo et al. (JP 2001-308262). Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 21, 22, 39-43 and 50 are patentable over Pai et al. (6,503,776).

Regarding Pai et al., the Examiner states:

Pai et al. ... specifically figure 8 show a semiconductor package comprising: ... a **second semiconductor chip 130 or 160 ... and an insulator 166 coupled to and covering the entire first surface of the second semiconductor chip ...** (Office Action, page 10, emphasis added.)

As set forth at page 9 of the amendments filed on June 16, 2004:

Pai et al.'s film adhesive layer 166 is coupled to the lower surface of the upper semiconductor chip 130, but is entirely inward of the bond pads of the lower semiconductor chip 110.

Accordingly, Pai et al. does not teach or suggest:

A semiconductor package comprising:
a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;
an adhesive layer coupled to the second surface of the first semiconductor chip;
a second semiconductor chip stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and
an insulator coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is attached to the first surface of the second semiconductor chip and the adhesive layer, and is vertically between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip,

as recited in amended Claim 21, emphasis added. Accordingly, Claim 21 is allowable over Pai et al. Claim 22, which depends

from Claim 21, is allowable for at least the same reasons as Claim 21.

For similar reasons, Pai et al. does not teach or suggest:

A semiconductor package comprising:
a substrate;
a first semiconductor chip coupled to the substrate, the first semiconductor chip having opposed first and second surfaces;
a second semiconductor chip having opposed first and second surfaces;
a first means coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip in a stack;
at least one pad formed on the second surface of the first semiconductor chip;
at least one first conductive wire connecting the at least one pad of the first semiconductor chip and the substrate;
at least one pad formed on the second surface of the second semiconductor chip;
at least one second conductive wire connecting the at least one pad of the second semiconductor chip and the substrate; and
an insulator attached to the first surface of the second semiconductor chip and the first means, and overlying both the first means and the at least one first conductive wire,

as recited in amended Claim 39, emphasis added. Accordingly, Claim 39 is allowable over Pai et al. Claims 40-43, which depend from Claim 39, are allowable for at least the same reasons as Claim 39.

For similar reasons, Pai et al. does not teach or suggest:

A semiconductor package comprising:
a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;
a plurality of conductive wires, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip;
a second semiconductor chip stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface,

and an opposite second surface that includes a plurality of pads;

an insulator coupled to and covering the entire first surface of the second semiconductor chip, said insulator being vertically between each of the conductive wires and the first surface of the second semiconductor chip;

an adhesive layer attached to the insulator and the second surface of the first semiconductor chip; and

a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is vertically between the pads of the second surface of the first semiconductor chip and the insulator,

as recited in amended Claim 50, emphasis added. Accordingly, Claim 50 is allowable over Pai et al.

For at least the above reason, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 21, 22, 39-42, 47, 50-64 are patentable over Mess et al. (2003/0137042) or Ball (5,952,725).

Claim 65 has been canceled without prejudice thus obviating the rejection of Claim 65.

Initially, Applicants respectfully submit that Mess et al. is not prior art with respect to the present application. Mess et al. is a divisional of application No. 09/886,593, filed on June 21, 2001. As set forth above, the present application is entitled to claim priority to **March 9, 2001**, which is before the filing date of **June 21, 2001** of application No. 09/886,593.

Should the Examiner disagree, Applicants respectfully request that the Examiner set forth the basis under which Mess et al. is prior art with respect to the present application.

With respect to Ball, the Examiner states:

the details of Ball (figure 9) specifically figure 8 show a semiconductor package comprising:
a first semiconductor chip 904 ... a second semiconductor chip 902 stacked over the second surface of the first semiconductor chip...; and **an insulator 908** coupled to and covering the entire first surface of the second semiconductor chip... (Office Action, page 11, emphasis added.)

The Examiner's statement is respectfully traversed. As shown in FIG. 9, the "insulator 908" is **entirely inward** of the bonding pads 906 of the "first semiconductor chip 904" and does not appear to **entirely** cover the lower surface of the "second semiconductor chip 902". More specifically, Ball teaches:

Notches or recesses 910 or chamfers 911 at the semiconductor substrate peripheries **expose bond pads 906** on lower substrate 904 ... (Col. 8, lines 25-27, emphasis added.)

Accordingly, Ball does not teach or suggest:

A semiconductor package comprising:
a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;
an adhesive layer coupled to the second surface of the first semiconductor chip;
a second semiconductor chip stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and
an insulator coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is attached to the first surface of the second semiconductor chip and the adhesive layer, and is vertically between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip,

as recited in amended Claim 21, emphasis added. Accordingly, Claim 21 is allowable over Ball. Claim 22, which depends from Claim 21, is allowable for at least the same reasons as Claim 21.

For similar reasons, Ball does not teach or suggest:

A semiconductor package comprising:
a substrate;
a first semiconductor chip coupled to the substrate, the first semiconductor chip having opposed first and second surfaces;

a second semiconductor chip having opposed first and second surfaces;

a first means coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip in a stack;

at least one pad formed on the second surface of the first semiconductor chip;

at least one first conductive wire connecting the at least one pad of the first semiconductor chip and the substrate;

at least one pad formed on the second surface of the second semiconductor chip;

at least one second conductive wire connecting the at least one pad of the second semiconductor chip and the substrate; and

an insulator attached to the first surface of the second semiconductor chip and the first means, and overlying both the first means and the at least one first conductive wire,

as recited in amended Claim 39, emphasis added. Accordingly, Claim 39 is allowable over Ball. Claims 40-42, which depend from Claim 39, are allowable for at least the same reasons as Claim 39.

For similar reasons, Ball does not teach or suggest:

A semiconductor package comprising:

a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;

a plurality of conductive wires, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip;

a second semiconductor chip stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads;

an insulator coupled to and covering the entire first surface of the second semiconductor chip, said insulator being vertically between each of the conductive wires and the first surface of the second semiconductor chip;

an adhesive layer attached to the insulator and the second surface of the first semiconductor chip; and

a sealing material covering the first and second semiconductor chips, **wherein a portion of the sealing**

material is vertically between the pads of the second surface of the first semiconductor chip and the insulator,

as recited in amended Claim 50, emphasis added. Accordingly, Claim 50 is allowable over Ball.

For similar reasons, Ball does not teach or suggest:

A semiconductor package comprising:
a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;
a plurality of conductive wires, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip;
a second semiconductor chip stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads;
an insulator coupled to and covering the entire first surface of the second semiconductor chip, said insulator being vertically between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip; and
an adhesive layer attached to the insulator and the second surface of the first semiconductor chip, the adhesive layer being entirely inward of the pads of the second surface of the first semiconductor chip,

as recited in amended Claim 51, emphasis added. Accordingly, Claim 51 is allowable over Ball. Claim 52, which depends from Claim 51, is allowable for at least the same reasons as Claim 51.

For similar reasons, Ball does not teach or suggest:

A semiconductor package comprising:
a first semiconductor chip having opposed first and second surfaces;
an adhesive layer coupled to the second surface of the first semiconductor chip;
a second semiconductor chip stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and
an insulator coupled to and covering the entire first surface of the second semiconductor chip, wherein the

insulator is attached to the adhesive layer and the first surface of the second semiconductor chip,

as recited in amended Claim 53, emphasis added. Accordingly, Claim 53 is allowable over Ball. Claims 54-64, which depend from Claim 53, are allowable for at least the same reasons as Claim 53.

For at least the above reason, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 43-46 and 60-62 are patentable over Kondo et al.

As set forth above, Kondo et al. is not prior with respect to present application. Accordingly, Claims 43-46 and 60-62 are allowable over Kondo et al.

For at least the above reason, Applicants respectfully request reconsideration and withdrawal of this rejection.

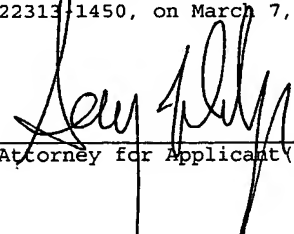
Conclusion

Claims 21-22, 39-47, 50-64 are pending in the application.

For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

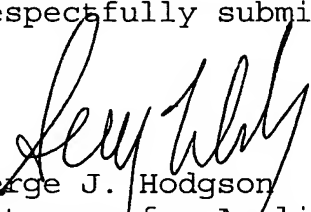
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 7, 2005



Attorney for Applicant(s)

March 7, 2005
Date of Signature

Respectfully submitted,


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